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EXAMINER	
ARCOS, CAROLINE H	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,178	YEUNG ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,10-15,19,39,40,44 and 46-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,10-15,19,39,40,44 and 46-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/06/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 7, 10-15, 19, 39-40, 44, 46-49 are pending for examination.

Claim Objections

2. Claims 46-47 are objected to because it is dependent on a cancelled claim 45. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-4, 7, 10-15, 19, and 39-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

i. The buffer level- claim 12 & 19.

b. The claim language in the following claims is not clearly understood:

ii. As per claim 1, it is unclear what is the relation between monitoring the state of the multi-threaded application and the buffer. what are the criteria for monitoring each. it is unclear what is meant by "state of multi threaded application (i.e. is it monitoring the buffer associated with the application?). Examiner interpret monitoring the state of the multi-threaded application is

monitoring the buffer associated with it as supported by the specification (abs.). it is unclear how the coordination of the thread dispatch increase execution overlap of the threads, It is unclear what is the criteria in the dispatch process that increase the execution overlap of the threads.

iii. As per claim 14, it has the same deficiency as claim 1.

iv. As per claim 39, it has the same deficiency as claim 1.Furthermore, Line 8, it is unclear what is meant by the multithreaded application running in a system buffer (i..e. is it executing in the system buffer?) Line 15, it is unclear whether "the buffer" is the same as "a system buffer" referred in line 8 (i.e. if it is the same it should be referred to it as "said system buffer).

Claim Rejections - 35 USC § 103

. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 11-14, 19, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1).

6. As per claim 1, Zaccarin teaches the invention substantially as claimed including a method, comprising:

monitoring a state of an application running in a system and a buffer associated with the multithreaded application , wherein each thread includes one or more activities to be executed by the system ([0013]; par. [0014], lines 15-23; par. [0015], lines 4-12; par. [0017]; par. [0019]; par. [0021]);

determining the buffer ([0013]; par. [0014]; par. [0015]; par. [0019]; par. [0020]); wherein at least one of the threads is associated with the application (par. [0013]; par. [0014]; par. [0015]);

coordinating the dispatch of threads of the multi-threaded application (par. [0013]-par. [0016]; par. [0019]-par. [0020]; wherein variation in processor frequency /voltage change the rate at which the threads are dispatched based on buffer level or application constraint);

dynamically adjusting one or more of the frequency or voltage applied to the processor based at least in part on the availability of the buffer and the coordination of the dispatch of the threads(par. [0015]-par. [0017]); and

dynamically adjusting the buffer size based at least in part on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads (par. [0015]; par. [0017]; par. [0019]).

7. Zaccarin does not explicitly teach determining the availability of a processor to perform simultaneous multi-threading, coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based at least in part on the availability of the buffer.

8. However, Cota- Robles teaches availability of a processor to perform simultaneous multi-threading and coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system (abs.; par. [0022]; par. [0025]; par. [0027]).

9. It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Cota-Robles because Cota-Robles teaching of SMT scheduling and coordinating the dispatching of the threads would increase system throughput and make better use of the processor.

10. The combined teaching does not explicitly teach the coordination of dispatching of threads of the multi-threaded application based at least in part on the availability of the buffer and determine the availability of a processor.

11. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching that in order the threads, one must determine first if there is any processor available for executing the threads and it is obvious according to Zaccarin teaching that changing the frequency /voltage of the processor based on the availability of the buffer is coordinating the dispatch of the threads by changing the dispatching rate based on the availability of the buffer as claimed.

12. As per claim 11, Zaccarin teaches said monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16;par. [0016], lines 10-12; par. [0018]).

13. As per claim 12, Zaccarin teaches said monitoring the buffer fullness levels includes, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0015], lines 8-16; Par. [0017]; par. [0018]).

14. As per claim 13, Zaccarin teaches said comparing the buffer level includes determining buffer overflow and buffer underflow conditions based at least in part, on the high level mark and the low level mark. (Par. [0015], lines 4-16; par. [0017], lines 4-15; par. [0018]-par. [0019]).

15. As per claim 14, it is the computer readable storage medium of the method claim 1. Therefore, it is rejected under the same rational.

16. As per claim 19, Zaccarin teaches monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer and wherein monitoring the buffer fullness levels includes, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16;

par. [0016], lines 10-12; par. [0017]; par. [0018]).

17. As per claim 39, Zaccarin teaches a system, comprising:

a memory to store data and instructions (fig. 4,42; par. [0042);

a processor ; said processor operable to perform instructions (fig. 4, 56);

monitor a state of an application running in a system buffer associated with the multi-threaded application; wherein each thread includes one or more activities to be executed by the system (par. [0013]- Par. [0014]);

determining the availability of a buffer ([0013]; par. [0014]; par. [0015]; par. [0019]; par. [0020]);

coordinating the dispatch of threads of the multi-threaded application (par. [0013]-par. [0016]; par. [0019]-par. [0020]; wherein variation in processor frequency /voltage change the rate at which the threads are dispatched based on buffer level or application constraint);

dynamically adjusting one or more of the frequency or voltage applied to the processor based at least in part on the availability of the buffer and the coordination of the dispatch of the threads(par. [0015]-par. [0017]); and

dynamically adjusting the buffer size based at least in part on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads (par. [0015]; par. [0017]; par. [0019]).

18. Zaccarin does not explicitly teach a processor coupled to said memory on a bus, said processor to include:

a bus unit to receive a sequence of instructions from said memory; an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions, determining the availability of a processor to perform simultaneous multi-threading, coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based at least in part on the availability of the buffer.

19. However, Cota- Robles teaches a bus unit to receive a sequence of instructions from said memory; an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions (fig.1; par. [0034]), availability of a processor to perform simultaneous multi-threading and coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system (abs.; par. [0022]; par. [0025]; par. [0027]).

20. It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Cota-Robles because Cota-Robles teaching of SMT scheduling and coordinating the dispatching of the threads would increase system throughput and make better use of the processor.

21. The combined teaching does not explicitly teach the coordination of dispatching of threads of the multi-threaded application based at least in part on the availability of the buffer and determine the availability of a processor.

22. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching that in order the threads, one must determine first if there is any processor available for executing the threads and it is obvious according to Zaccarin teaching that changing the frequency /voltage of the processor based on the availability of the buffer is coordinating the dispatch of the threads by changing the dispatching rate based on the availability of the buffer as claimed.

23. Claims 2-4, 15, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1), and further in view of Kling et al. (US 6,662,203 B1).

24. As per claim 2, the combined teaching of Zaccarin and Cota-Robles does not explicitly teach controlling the dispatch of the threads of the multi-threaded application in the system includes assessing execution readiness of the one or more activities of each thread.

25. However, Kling teaches said controlling the dispatch of the threads of the multi-threaded application in the system includes assessing execution readiness of the one or more activities of each thread. (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Cota-Robles and kling because Kling teaching of accessing readiness of the one or more activities improve system dispatching techniques and

increase efficiency in dispatching technique of the system since one would only be dispatching ready activities only which improve the performance of the system.

27. As per claim 3, Kling teaches said controlling the dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

28. As per claim 4, Zaccarin teaches the first and second activities are from one or more applications (par. [0012]; par. [0021]).

29. The combined teaching of Zaccarin, and Cota-Robles does not explicitly teach that a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

30. However, Kling teaches a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

31. As per claim 15, it is the computer readable medium of the method claim 3. Therefore it is rejected under the same rational.

32. As per claim 40, the combined teaching of Zaccarin and Cota-Robles does not explicitly teach that said controlling the dispatch of the threads of the multi-threaded application includes delaying a ready- to-be-dispatched thread from being dispatched.

33. However, Kling teaches said controlling the dispatch of t of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched thread from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1- 15; fig. 5).

34. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Cota-Robles and kling since Kling teaching of delaying a ready-to-be- dispatched thread from being dispatched would improve system throughput and increase efficiency of system resource usage.

35. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1), as applied to claim 1 above and further in view of Myers et al. (US 4,811,208).

36. As per claim 7, Zaccarin teaches coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components (par. [0013]-par. [0020]).

37. The combined teaching of Zaccarin and Cota-Robles does not explicitly teach teaches the configurable hardware components including arithmetic logic unit (ALU), and registers in the system, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components.

38. However, Myers teaches the configurable hardware components including arithmetic logic unit (ALU), and registers in the system, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components (abs.; col. 1, lines 35-56; col. 3, lines 1-65).

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin , Cota-Robles and Myers because Myers teaching expand the configurable hardware in the system.

40. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1) and in view of Myers et al. (US 4,811,208) as applied to claim 7 above, and further in view of Jain et al. (US 2002/0188884 A 1).

41. As per claim 10, the combined teaching of Zaccarin , Cota-Robles and Myers does not explicitly teach that said increasing or decreasing the resources in the system includes powering

on or powering off at least a portion of circuitry in the system.

42. However, Jain teaches said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system (par. [0040]; claim 1).

43. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Cota-Robles, Myers and Jain because Jain teaching of said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system would improve system energy consumption and increase efficiency.

44. Claim 44, 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Yavatkar et al. (US 2003/0137945 A1) and further in view of Armstrong et al. (US 2004/0216113 A1), and further in view of Kling et al. (US 6,662,203 B1).

45. As per claim 44, Zaccarin teaches a system, comprising:

processor (fig. 4, 56);

a resource manager coupled to processor (fig. 4);

the resource manager is to monitor states of a multi-threaded application running in the system, the states of the application including buffer fullness levels of one or more buffers used

by the application,(par. [0013]; par. [0014]; par. [0015]; par. [0017]; par. [0021]).

46. Zaccarin does not explicitly teach a multi-threading processor; and the resource manager is to further monitor states of the threads in the system for execution readiness and the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the threads in the system and change the execution readiness of a thread from ready state to a queued state to increase subsequent thread execution overlap with execution of another thread based at least in part on the buffer fullness levels.

47. However, Yavatkar teaches the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the one or more threads in the system (fig. 4; par. [0018]; par. [0020]; [0021]).

48. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Yavatkar because Yavatkar teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based at least on the state of the application and the state of the threads and taking into consideration the buffer level would be well known to one of ordinary skill in the art of due to monitoring buffer levels, managing the energy of the processor taking into the account the state of the threads that can be manipulated in adjusting the buffer levels.

49. The combined teaching Zaccarin and Yavatkar does not explicitly teach a multi-threading processor and the resource manager is to further monitor states of a plurality of threads in the system for execution readiness and change the execution readiness of a thread from ready state to a queued state to increase subsequent thread execution overlap with execution of another thread based at least in part on the buffer fullness levels.

50. However, Armstrong teaches a multi-threading processor (par. [0004]; par. [0006]; par. [0011]).

51. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Armstrong because Armstrong teaching of simultaneous multi-threading which increase overlapping of multiple threads execution at one time.

52. The combined teaching of Zaccarin, Yavatkar and Armstrong does not explicitly teach the resource manager is to further monitor states of a plurality of threads in the system for execution readiness and change the execution readiness of a thread from ready state to a queued state to increase subsequent thread execution overlap with execution of another thread based at least in part on the buffer fullness levels.

53. However, kling teaches the resource manager is to further monitor states of a plurality of threads in the system for execution readiness (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3,

lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

54. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Armstrong and Kling because Kling teaching of monitor states of one or more threads in the system for execution readiness would improve dispatching and scheduling techniques and system performance by monitoring ready thread to dispatch them.

55. The combined teaching of Zaccarin, Yavatkar and Armstrong and Kling does not explicitly teach and change the execution readiness of a thread from ready state to a queued state to increase subsequent thread execution overlap with execution of another thread based at least in part on the buffer fullness levels.

56. However, it would be obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching of Zaccarin, Yavatkar and Armstrong and Kling and especially Kling of delaying execution of threads (change from ready to queued) in order to execute them in a batch wise is change the execution readiness of a thread from ready state to a queued state to increase subsequent thread execution overlap with execution of another thread as claimed and Zaccarin and Yavatkar teaching of monitoring buffer fullness and adjusting processor frequency based on the fullness of the buffer which affect the rate at which the thread is dispatched, it would be obvious to incorporate the teaching of Kling in delaying the

dispatch as a way to control the buffer fullness.

57. As per claim 46, Kling teaches change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58- col. 4, lines 1- 24; col. 9, lines 38-col. 10, lines 1-15).

58. The combined teaching of Zaccarin, Yavatkar and Armstrong and Kling does not explicitly teach that the change is to increase subsequent system idle time when there is no thread execution. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Kling teaching of batch system and changing from ready to queued state that beside increasing the efficiency in using the system resource, it is increasing subsequent system idle time when there is no thread execution which improve the system throughput by processing the threads in a parallel at once.

59. As per claim 47, Zaccarin teaches the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to the one or more buffers (par. [0013]; par. [0014]; par. [0015]par.[0017]).

60. As per claim 48. Zaccarin teaches an apparatus, comprising:

logic to monitor states of an application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28; par. [0015], lines 4-16;

par. [0017], lines 4-15); and to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more buffers are in a critical stage (par. [0017]-par. [0019]; and a memory to store the logic (par. [0024]).

61. Zaccarin does not explicitly teach a processor capable of simultaneous multi- threading, logic to adjust resources available in the system depending on the state of the application and/or the states of the threads in the system and logic to monitor states of a plurality of threads in the system for execution readiness.

62. However, Yavatkar teaches logic to adjust resources available in the system depending on the state of the application and/or the states of the threads in the system fig. 4; par. [0018]; par. [0020]; [0021]).

63. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Yavatkar because Yavatkar teaching of dynamically adjusting one or more of the frequency or the voltage applied to the processor based taking into consideration the buffer level would be well known to one of ordinary skill in the art of due to monitoring buffer levels, managing the energy of the processor taking into the account the state of the threads that can be manipulated in adjusting the buffer levels.

64. The combined teaching Zaccarin and Yavatkar does not explicitly teach a processor capable of simultaneous multi-threading, and logic to monitor states of a plurality of threads in

the system for execution readiness.

65. However, Kling teaches logic to monitor states of one or more threads in the system for execution readiness (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

66. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar and Kling because Kling teaching of monitoring the execution readiness of one or more thread would improve Zaccarin system performance and dispatching techniques by knowing that one or more threads are ready to be executed, one would be able to take the steps necessary to dispatch them.

67. The combined teaching of Zaccarin, Yavatkar and Kling does not explicitly teach a processor capable of simultaneous multi-threading. However, Armstrong teaches a processor capable of simultaneous multi-threading (par. [0004]; par. [0006]; par. [0011]).

68. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Yavatkar, Kling and Armstrong because Armstrong teaching of simultaneous multi-threading which increase overlapping of multiple threads execution at one time.

69. As per claim 49, Kling teach logic to change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4,

lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

70. The combined teaching of Zaccarin, Yavatkar, Kling and Armstrong does not explicitly teach that the change in state is when it is determined that there is no other thread running or ready to be dispatched.

71. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching and especially Kling teaching that the ready threads are moved to wait queue until the batch is complete to be dispatched so it would have been obvious that the first thread in the ready queue is moved to the wait queue until other ready threads becomes ready and join the first thread in the wait queue, when they will be dispatched.

Response to Arguments

72. Applicant's arguments with respect to claims 1-4, 7, 10-15, 19, and 39-40, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

73. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 7155600 B2 teaches Method and logical apparatus for switching between single-threaded and multi-threaded execution states in a simultaneous multi-threaded (SMT) processor.
US 7213135 B2 teaches Method using a dispatch flush in a simultaneous multithread processor to resolve exception conditions.

74. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

75. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

76. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

77. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

78. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Caroline Arcos/
Examiner, Art Unit 2195